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APPLICATION NUMBER: *60/372,132*
FILING DATE: *April 12, 2002*

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PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

Express Mail Label No. EL915426681US

INVENTOR(S)		
Given Name (first and middle [if any])	Family Name or Surname	Residence (City and either State or Foreign Country)
Ionel D.	Jitaru	Tucson, Arizona

☐ *Additional inventors are being named on the _____ separately numbered sheets attached hereto*

TITLE OF THE INVENTION (500 characters max)

SOFT SWITCHING HIGH EFFICIENCY FLYBACK CONVERTER

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ENCLOSED APPLICATION PARTS *(check all that apply)*

☒ Specification *Number of Pages* 7
☒ Drawing(s) *Number of Sheets* 7
☐ Application Data Sheet. See 37 CFR 1.76
☐ CD(s), Number
☒ Other (specify) Postcard

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT

☐ Applicant claims small entity status. See 37 CFR 1.27.
☒ A check or money order is enclosed to cover the filing fees
☐ The Commissioner is hereby authorized to charge filing fees or credit any overpayment to Deposit Account Number:
☐ Payment by credit card. Form PTO-2038 is attached.

FILING FEE AMOUNT ($): $160.00

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

☐ No.
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Respectfully submitted,

SIGNATURE _____ Date 4/12/02

TYPED or PRINTED NAME Thomas D. MacBlain REGISTRATION NO. *(if appropriate)* 24,583

TELEPHONE 602-530-8088 Docket Number: 14609-0004

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FEE TRANSMITTAL for FY 2002

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TOTAL AMOUNT OF PAYMENT ($) 160

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	Jitaru
Examiner Name	
Group Art Unit	
Attorney Docket No.	14609-0004

METHOD OF PAYMENT *(check all that apply)*

XXX ☐ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☐ Deposit Account:

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	740	201	370	Utility filing fee	
106	330	206	165	Design filing fee	
107	510	207	255	Plant filing fee	
108	740	208	370	Reissue filing fee	
114	160	214	80	Provisional filing fee	160

SUBTOTAL (1) ($) 160

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

	Extra Claims		Fee from below	Fee Paid
Total Claims	-20** =	X		=
Independent Claims	- 3** =	X		=
Multiple Dependent				=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	84	202	42	Independent claims in excess of 3
104	280	204	140	Multiple dependent claim, if not paid
109	84	209	42	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

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FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for *ex parte* reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension for reply within second month	
117	920	217	460	Extension for reply within third month	
118	1,440	218	720	Extension for reply within fourth month	
128	1,960	228	980	Extension for reply within fifth month	
119	320	219	160	Notice of Appeal	
120	320	220	160	Filing a brief in support of an appeal	
121	280	221	140	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,280	241	640	Petition to revive - unintentional	
142	1,280	242	640	Utility issue fee (or reissue)	
143	460	243	230	Design issue fee	
144	620	244	310	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Processing fee under 37 CFR 1.17(q)	
126	180	126	180	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	740	246	370	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	740	249	370	For each additional invention to be examined (37 CFR § 1.129(b))	
179	740	279	370	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid SUBTOTAL (3) ($)

SUBMITTED BY

Name (Print/Type)	Thomas D. MacBlain	Registration No. (Attorney/Agent)	24,573	Complete (if applicable) Telephone	602-530-8088
Signature				Date	4/12/02

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Docket No. 14609-0004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Ionel Jitaru

Serial No.:

Filed: Herewith

For Provisional Patent Application Entitled: SOFT SWITCHING HIGH EFFICIENCY FLYBACK CONVERTER

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on

4/12/02
Date

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Suzanne Shields

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997394/14609.0004

SOFT SWITCHING HIGH EFFICIENCY FLYBACK CONVERTER

Field of the Invention

This invention relates to a driving/synchronization technique used to achieve zero voltage switching and regulate the output of DC-DC converters.

Background of the Invention

In order to miniaturize power supplies, the control for power supplies has to be simplified. Another method is to increase switching frequencies to reduce capacitive and magnetic elements. In today's and future power supplies there is a need to reduce the amount of components needed to control the power supply. Among the greatest challenges is communication across the isolation boundary. Several techniques exist. There are opto-couplers, transformers, radio frequency devices, etc. This invention describes a technique using the same transformer that is used for power conversion. The technique is not by sending complicated encoded information but by actually changing the effective duty cycle from the secondary.

One implementation of this invention will be shown as a self-oscillating flyback converter. This technique can be used with other topologies but the flyback converter is the easiest topology to illustrate the idea. Plus this topology offers reduced number of control parts, which illustrates the advantage of this invention. Fig. 2A shows a typical self-oscillating flyback converter where an input voltage source 16 supplies a primary winding 18 of a transformer 32 in series with a primary switch 8. Its turn OFF command is controlled by a combination of a transistor 22 and positive feedback from a winding 20, a capacitor 14 and a gate resistor 12. Turn ON is primarily controlled with the same winding circuit, plus a resistor 10 provides turn

ON at initial startup. The transistor 22 is turned on if the current through a resistor 24 is sufficiently high when the switch 8 is on. During the times the switch 8 is off, it provides a voltage 25 alternating in polarity to the output circuit. When the output load circuit comprising a load 31 and a filtering capacitor 30 is coupled, during the OFF time of the switching period, current flows through secondary winding 26 of the transformer 32 and through a diode D1 to the output load 31 and the filter capacitor 30.

In Fig. 2B are displayed the voltages and currents versus time waveforms for the self-oscillating flyback circuit parameters, i.e.: primary gate voltage 34 of the switch 8, primary drain voltage 36 of the switch 8, and transformer primary winding current 40 and secondary winding current 38.

A first, main drawback of this approach is that there is no regulation. The control is simple but adding regulation will add complexity and parts. Plus to regulate the output well an opto-coupler has to be added. A second drawback is that for low output voltages the diode has a large relative forward voltage drop. A third drawback is the primary switch 8 does not have zero voltage switching in all situations. By adding a synchronous rectifier in place of the diode D1, to serve as a switch in the secondary circuit, the second drawback can be avoided. This could introduce other problems including cross conduction. Controlling this synchronous rectifier correctly, the first two drawbacks can be eliminated plus cross conduction can be avoided.

Summary of the Invention

The invention employs a concept of pushing back energy to the input circuit. In a sense the secondary can change the effective duty cycle by making the off time longer. This regulates the output. This extra energy can be put to good use in the primary by providing zero voltage

switching. This also prevents cross conduction. Since zero volt switching can prevent switching losses at higher frequencies, the size of the converter can further be reduced.

The timing of synchronous and primary MOSFETS serving as the synchronous rectifier and the primary switch is important. The invention also provides a simple method of achieving this idea and a general methodology.

This concept leads to a general concept in a flyback converter that is bi-directional converter. In this converter, by controlling MOSFET ON and OFF times correctly, zero voltage switching can be accomplished on both MOSFETS. The algorithm to accomplish this is given.

Objects of this invention are, among others:

1. A driving technique or algorithm that accomplishes zero voltage switching in both the primary and secondary switching devices.

2. A regulation technique using said algorithm in the primary, secondary or both.

3. A method of implementing detection and regulation of the driving technique by using winding detection, current detection, or ripple detection in the secondary side of a DC-DC converter.

The above and further objects and advantages of the invention will be better understood from the following detailed description of at least one preferred embodiment of the invention, taken in consideration with the accompanying drawings.

Brief Description of the Drawings

Figure 1A is a semi-generalized schematic of a self-oscillating flyback converter utilizing the concept according to this invention;

Figure 1B plots the waveforms of the new concept converter according to Fig. 1A;

Figure 2A is a schematic of a prior art self-oscillating flyback converter;

Figure 2B plots the waveforms of a typical self-oscillating flyback converter as shown in Fig. 2A;

Figure 3 is a schematic of one further implementation of the invention;

Figure 4A is a schematic partially in block diagram form, of a generalized flyback converter according to the invention; and

Figure 4B plots the waveforms of the generalized flyback converter of Fig. 4A.

Detailed Description

A semi-general illustration of the proposed concept applied to a self-oscillating flyback converter is illustrated in Fig. 1A with corresponding waveforms shown in Fig. 1B. Assume the converter is just powered up by applying an input voltage Vin from the source 56. A resistor 52 charges a capacitor 57 and, through resistor 58, a gate capacitance of a MOSFET M1 acting as a switch 62. MOSFET M1 turns on when its gate threshold is reached. Voltage is applied to the primary winding 66 as the primary drain voltage 84 starts to go down at point T_0 as illustrated in Fig. 1B. This in turn produces a voltage on winding 64 which increases the primary gate voltage 82 on the MOSFET M1 further, which saturates the device. Primary current 86 ramps up at a rate dependent on the inductance of the primary winding 66. When the primary current 86 reaches a level that produces a drop across resistor 65 larger than its V_{be}, a transistor 60 turns on, which starts to discharge the primary gate voltage 82 of the MOSFET M1 at time T_1. When MOSFET M1 starts to turn off, the primary drain voltage 84 of MOSFET M1 starts to rise. This changes the voltage on the positive feedback winding 64 to a lower value, which further shuts off the MOSFET M1, more quickly producing a fast turn off. Once the MOSFET M1 is completely off the current built up in primary winding 66 and transformer 67 must flow through an available winding. When the voltage on secondary winding exceeds the output voltage, the secondary

current 88 starts to flow through the body diode 69 of MOSFET M2. A control circuit 75 for the MOSFET M2 is made up of a comparitor 76, a reference voltage source 78 connected from the output to one input of the comparitor, and a voltage divider 74, 80 connected to the other comparitor input. The reference voltage source 78 provides a fixed voltage V_{ref} across it. It may be a small battery or equivalent. The control circuit 75 on the secondary turns on MOSFET M2 once it detects a negative voltage at the drain of the MOSFET M2. This reduces the drop across M2. The current decays with constant negative slope in the secondary from time T_1 to time T_2 as it delivers energy to the output. The current eventually crosses zero at time T_2. Then the secondary current 88 reverses, which flows into the drain of the MOSFET M2 producing a positive voltage drop. When there is a sufficient amount of positive voltage at the drain of the MOSFET M2 detected by the divider formed by a pair of resistors 80 and 74, a control capacitor 76 turns off the MOSFET M2 at time T_3. So, at time T_3 the secondary current 88 was negative. Reference 78 is used to regulate the output voltage, which modulates this turn off time. If the output voltage is low the MOSFET M2 is turned off right at zero, if the output is higher than expected the MOSFET 72 is left on longer, which pushes more current back. By changing the amount of current going back, the secondary side of the converter can regulate the output. When the MOSFET M2 turns off the current that was pushed back (negative secondary current 88), the transformer reverses the primary winding 66. The primary winding starts to move charge out of the MOSFET M1 drain back into the input source 56, which starts to lower the primary drain voltage 84 at time T_3. The resistor 58 provides a delay while this is happening such that the MOSFET M1 turns on when its drain reaches zero. The greater the current pushed back to the primary from the secondary the faster the drain of the MOSFET M1 will fall. Once M1 is turned on, the whole process repeats. Both MOSFETS M1 and M2 experienced zero voltage turn on.

Another simple control is illustrated in Fig. 3. All the primary components are the same, but the control of the MOSFET M2 is accomplished with an extra winding. The MOSFET M2 itself regulates the voltage by its intrinsic turn-on threshold. Resistors 112, 114, and a winding 116 turns ratio help to adjust the output voltage. The advantage of this topology is that it is very simple. The disadvantage is that the MOSFET M2 is not very well turned on. But for low power small converters it is very useful.

To illustrate the concept and timing algorithm a more general schematic is shown in Fig. 4A with waveforms in Fig. 4B. The converter could be bi-directional. Lets assume we are processing energy from left to right. Control C1 turns on MOSFET M1 at T_o (in Fig. 4B) at a time after it detects a negative current 222 flowing through the current sensor CS_1 plus a delay so that the drain of the MOSFET M1 has reached zero. It then decides, only when the current 222 has become positive, based on the input voltage or a fixed time, and/or winding voltages, to shutoff M1. The algorithm for C1 is turned on at zero voltage on the drain of M1 and there is a negative current 222, and as long as the current is negative the MOSFET M1 must remain on; then when the current is positive it is allowed to decide how long to leave the MOSFET M1 on. The decision on how long to remain on is based on either the input voltage, output voltage, winding voltages, or peak current 222. The same algorithm applies to the secondary side controller C2. Control C2 uses current sensor CS_2 with the same algorithm as control C1. The current in the MOSFET M2 is monitored. M2 is turned on when its drain is zero and there is a negative current 224 through it. Again the decision to turn off is allowed only when the current 224 is positive. The amount of time the current is positive is again up to the power direction and the regulation method used. The way the regulation of the input or the output is accomplished determines the power direction flow. As long as the base algorithm is followed both switches

have zero voltage switching. In Fig. 4B the waveforms are shown. It can be seen that current through M1 has the same basic shape as current in M2. The waveforms show power flow from primary to secondary since the average of the current 222 in M1 is positive. The gate voltage of M1 and the gate voltage of M2 are primarily inverted except for delays needed to achieve zero voltage switching. At T_0 M1 is turned on, at T_1 the current 222 crosses zero and after that the control C1 decides when to turn off M1. At T_2 the control C1 turns off M1 with a low gate voltage 226. After a short delay, to wait for zero volts on the drain of M2, M2 is turned on by the control C2 applying to the gate of M2 the voltage 228 since it detected a negative current through CS_2. At time T_3, the current 224 crosses zero and again the decision to turn off is allowed only when the current 224 is positive. At time T_4 the secondary controller C2 decides to shut off based on one or more of the input voltage 200, output voltage 212, winding voltage 208, or current level in CS_2.

The foregoing descriptions of at least one preferred embodiment are exemplary and not intended to limit the claimed invention. Obvious modifications that do not depart from the spirit and scope of the invention as claimed will be apparent to those skilled in the art.

Claim

1. In a DC – DC converter having a primary circuit connected to a primary winding of a transformer and a secondary circuit connected to a secondary winding of a transformer, an input connection to the primary circuit adapted to receive an input voltage and a load connection to the secondary circuit adapted to connect an output voltage to a load, a first signal-controlled semiconductor switching device in the primary circuit connected in current controlling relation to the primary winding of the transformer, and a positive feedback path including a further winding of the transformer in the primary circuit, the feedback path connected to apply a control signal in controlling relationship to the first signal-controlled semiconductor switching device; the improvement comprising:

a) a second signal-controlled semiconductor switching device in the secondary circuit connected in current switching relationship to the secondary winding of the transformer,

b) a control circuit connected in controlling relation to the second signal-controlled semiconductor switching device in the secondary circuit, the control circuit being connected to produce a control signal dependent on a relationship between the output voltage of the converter and a reference voltage,

c) a reference voltage source providing the reference voltage, and

d) the control circuit having an output voltage-dependent, voltage-supplying circuit connection to the load connection and a connection to the reference voltage source, whereby the control circuit effects energy transfer back to the primary circuit when output voltage rises so as to alter the duty cycle of the first signal-controlled semiconductor switching device to thereby regulate output voltage.

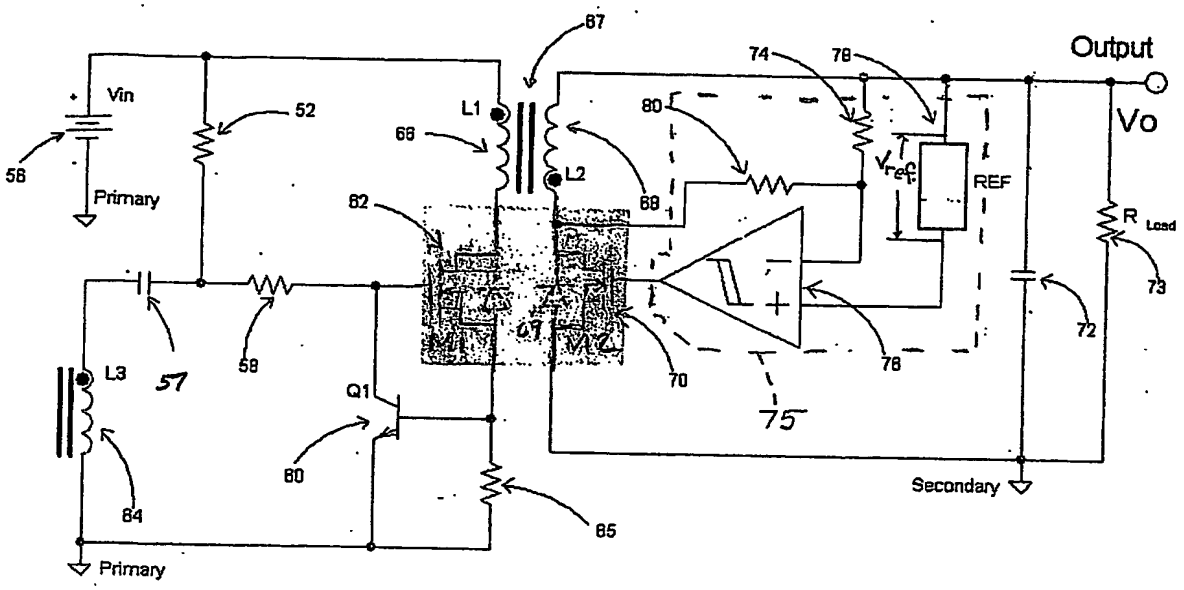


Figure 1A

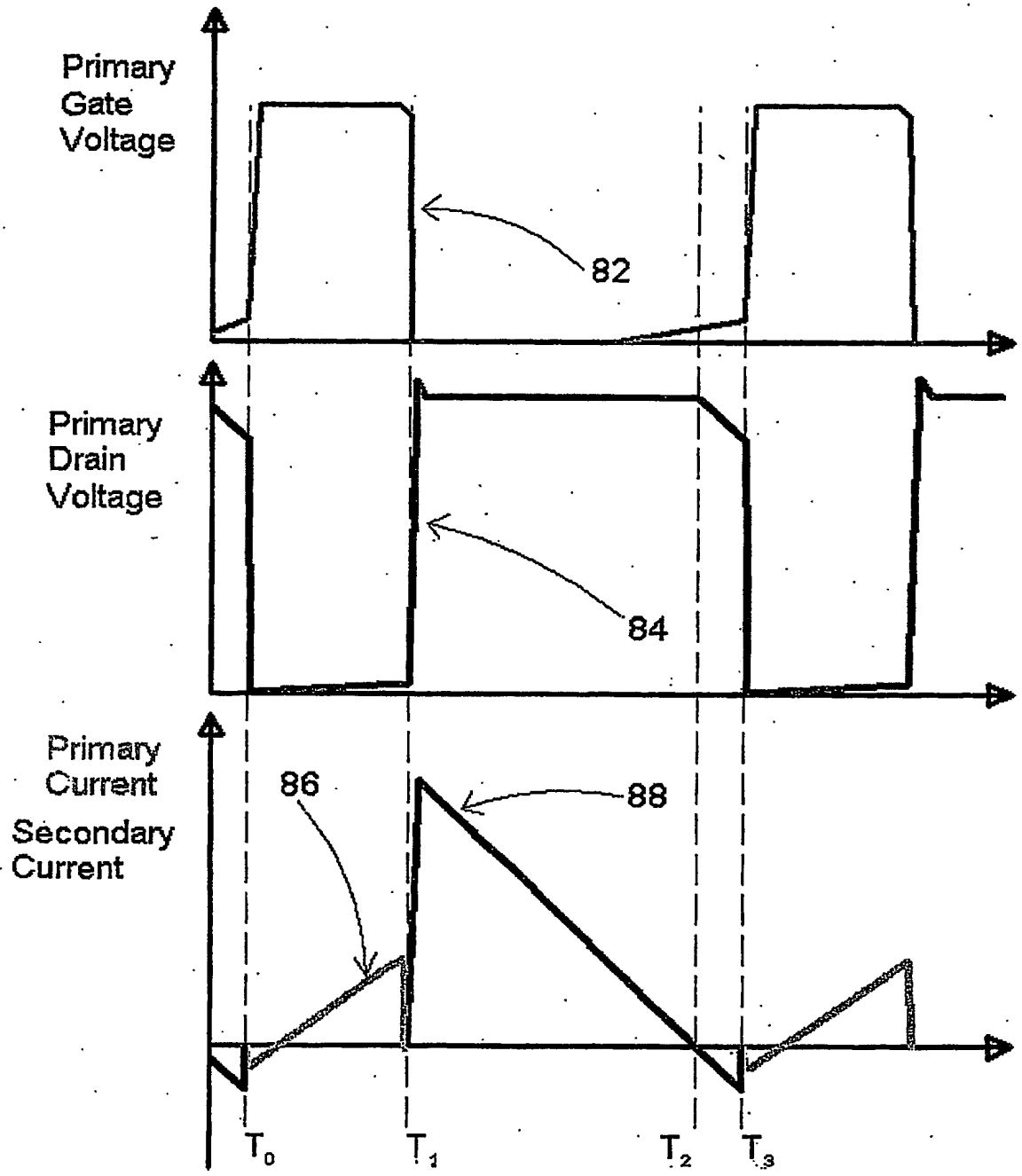
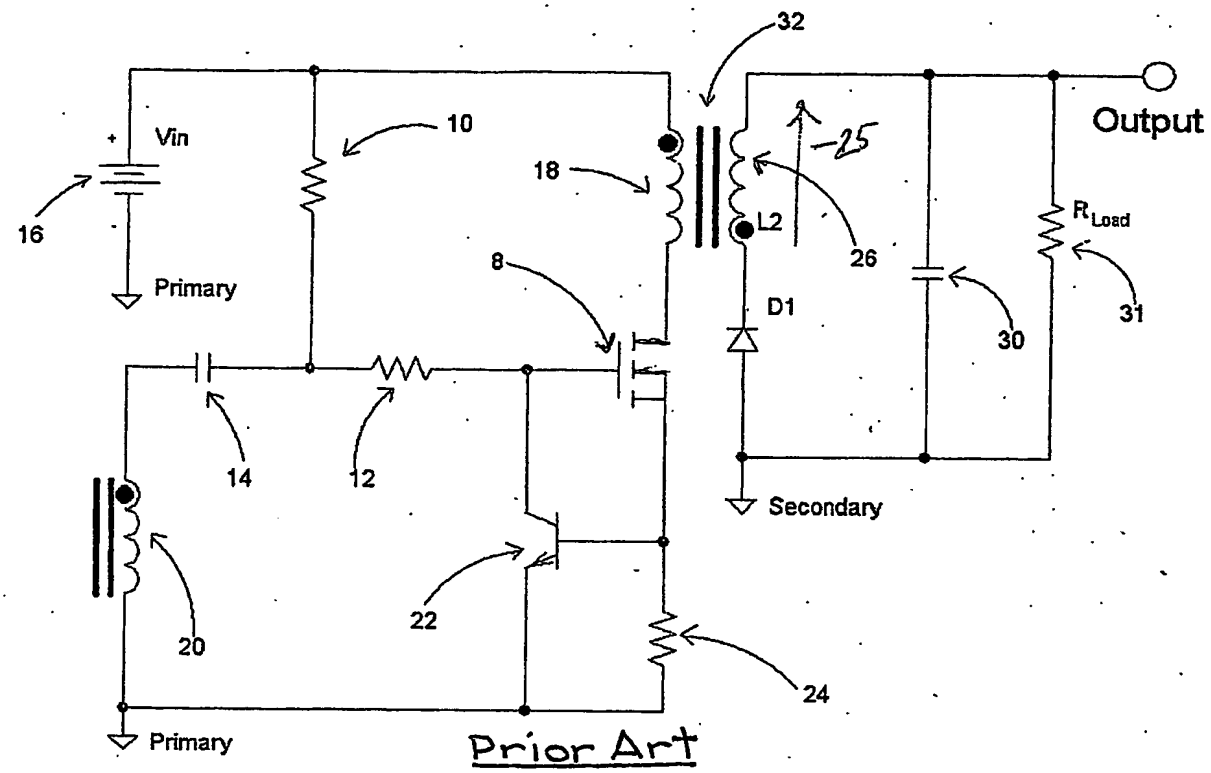
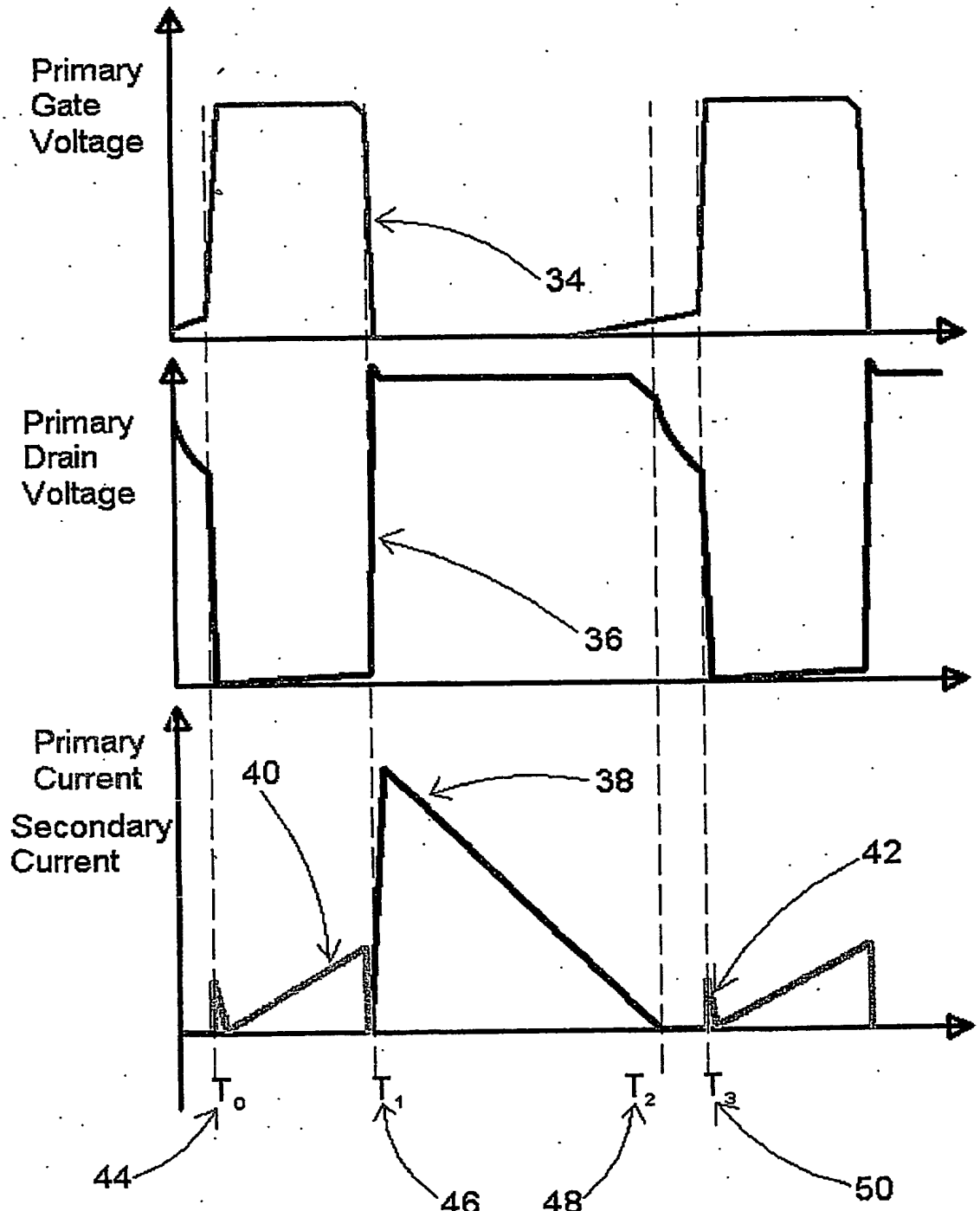


Figure 1B



Prior Art

Figure 2A



Prior Art
Figure 2B

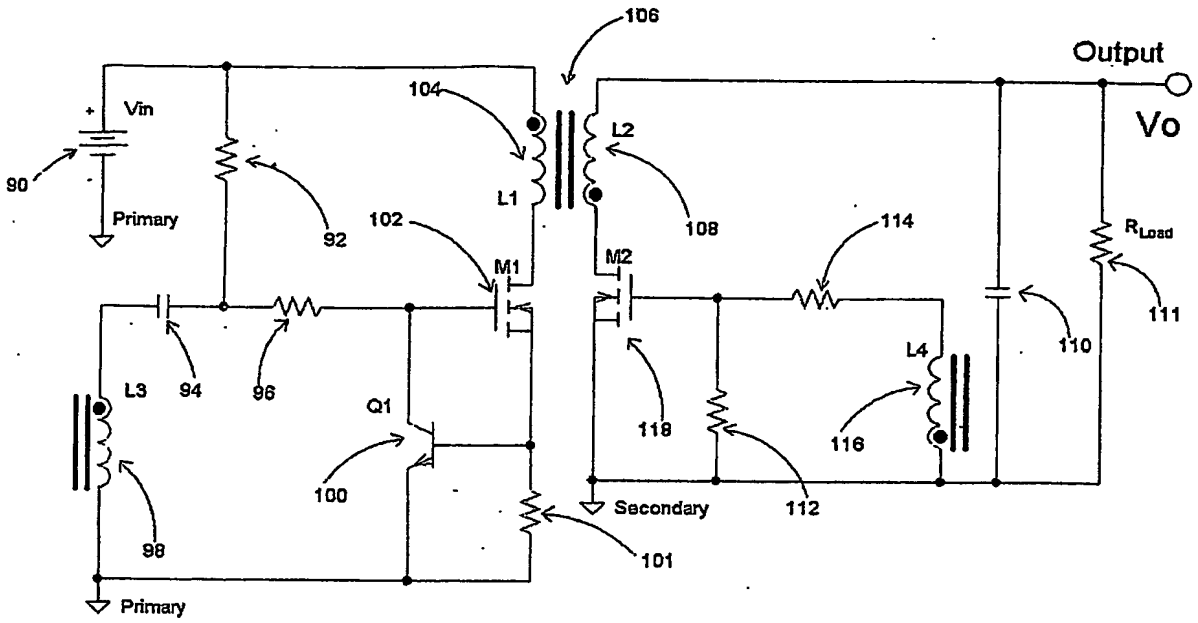


Figure 3

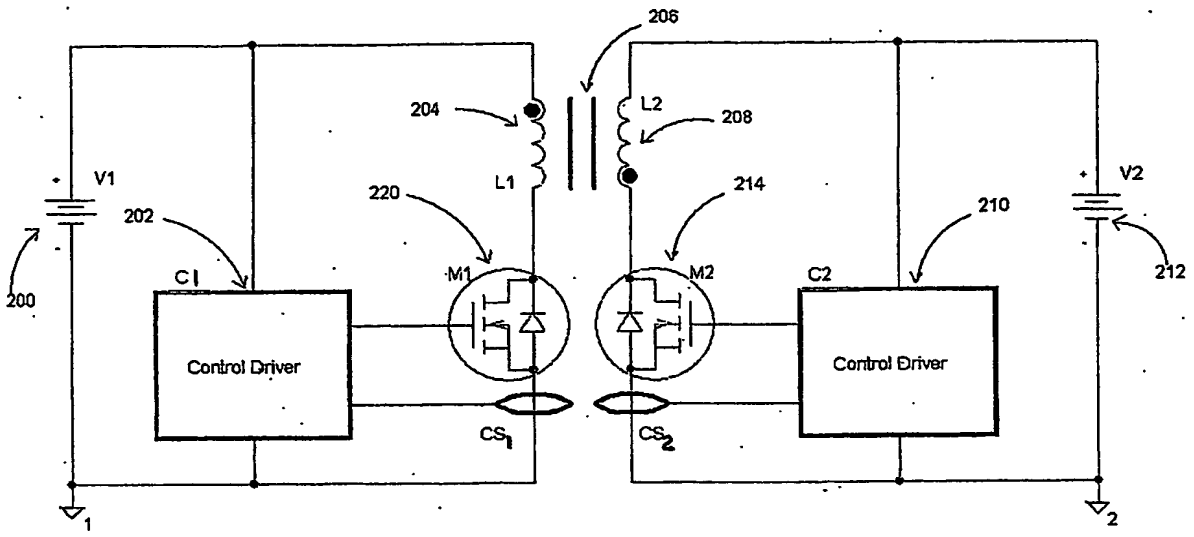


Figure 4A

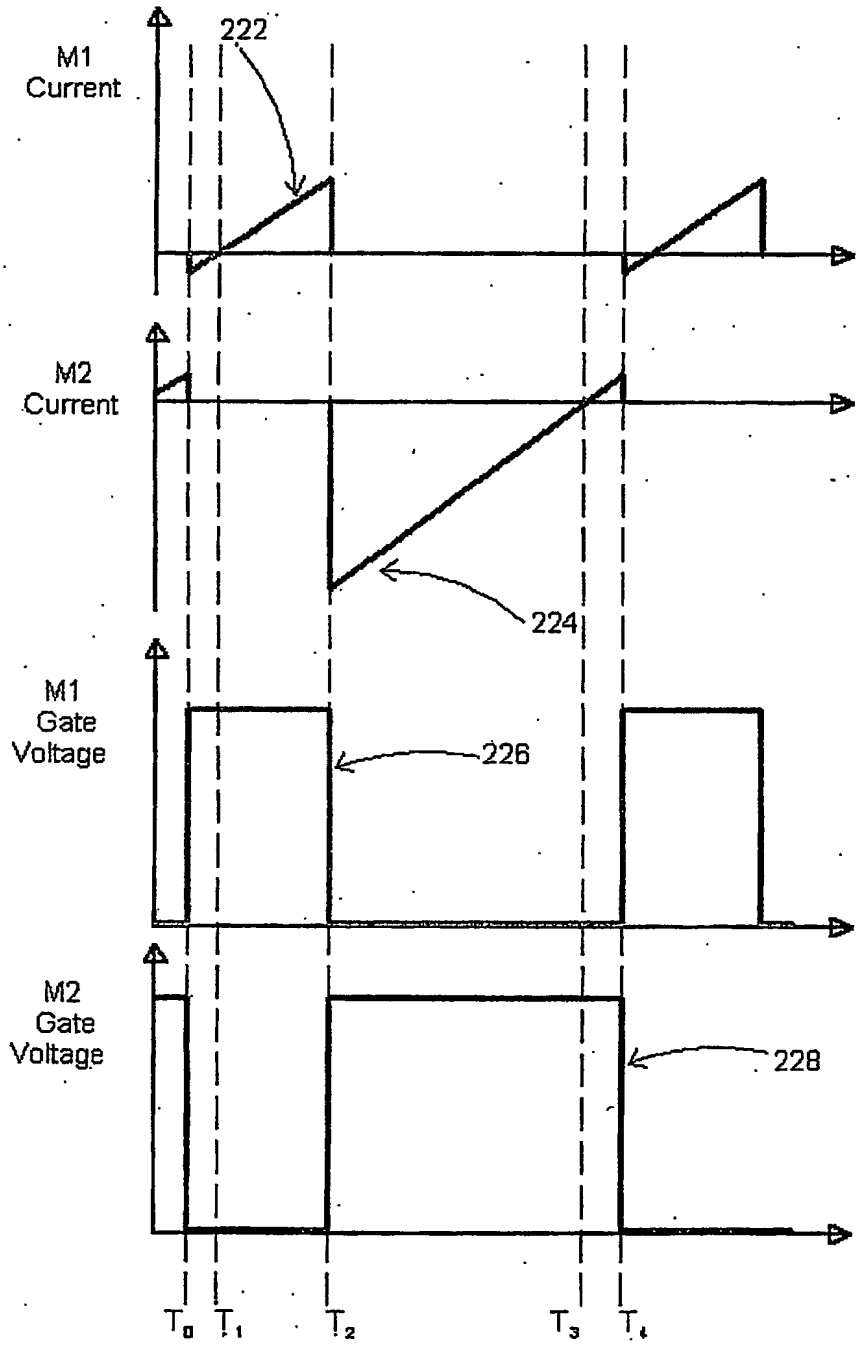

M1
Current
222
M2
Current
224
M1
Gate
Voltage
226
M2
Gate
Voltage
228
T0
T1
T2
T3
T4

Figure 4B